REMARKS

The Office Action dated February 22, 2008 has been received and considered. Reconsideration of the outstanding rejection in the present application is respectfully requested based on the following remarks.

Obviousness Rejection of Claims 13, 15-29, 31-40, 43-50, and 52-54

At page 2 of the Office Action, claims 13, 15-29, 31-40, 43-50, and 52-54 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Eifrig (US 6,748,020) in view of Pian (US 6,366,614). This rejection is respectfully traversed.

Obviousness of Separate Processors

Independent claims 13, 44, and 53 recite subject matter directed to a first processor and a second processor and their respective functionality/operations. For each of claims 13, 44, and 53, the Office asserts that element 10 ("parsing/demux 10") of FIG. 1 of Eifrig represents the claimed "first processor" feature and that element 30 ("core transcoding 30") of FIG. 1 of Eifrig represents the claimed "second processor" feature. *See Office Action*, pp. 2, 5, and 6. As discussed in greater detail at pages 9-12 of the Response filed May 7, 2007 (hereinafter, "the First Response") and at pages 9-11 of the Response filed November 20, 2007 (hereinafter, "the Second Response"), and as acknowledged by the Office at page 6 of the Office Action, Eifrig fails to disclose that element 10 and element 30 are implemented as separate processors. In fact, Eifrig expressly teaches that element 10 and element 30 are implemented at the same Very Long Instruction Word (VLIW) core. *See, e.g., Eifrig*, col. 4, lines 6-33 ("a) MPEG transport stream decoding (on VLIW core)(10) [. . .] c) Core transcoding (on VLIW core)(30) [. . .]")(emphasis added). As also discussed in the First Response and the Second Response, one of ordinary skill in the art will recognize that the parsing/demux (element 10) and the corresponding core transcoder (element 30) conventionally are implemented together as a single processor.

The Office responds to the failure of Eifrig to contemplate separate processors by turning to Pian, which the Office alleges as teaching "in figure 1, elements 10 and 12, that a preprocessor and an encoder can be constructed as two separate processors. And, therefore, it would have

been obvious . . . to modify the system of Eifrig et al by constructing a preprocessor and [a] transcoder as two separate processors as taught by Pian et al as a matter of various variance [sic] . . ." *Office Action*, pp. 6-7. The Applicants respectfully disagree. Contrary to the Office's assertions, nowhere does Pian disclose or suggest that the preprocessor 10 and the encoder 12 are constructed as separate processors. For example, while the preprocessor 10 and the encoder 12 as represented in FIG. 1 of Pian using different boxes, nowhere does Pian attribute any particular meaning to this use of different boxes as being associated with separate processors, and one of ordinary skill in the art would correctly interpret the use of different boxes for the preprocessor 10 and the encoder 12 merely as a common format for partitioning the different functions provided by each. Further, at the passage at col. 4, lines 38-42, Pian teaches that the "encoder 12 and rate controller 14[] are implemented in a microprocessor or digital signal processor programmed to provide the functions as described" but fails to disclose or even suggest that the preprocessor 10 is implemented in a second processor separate from the "microprocessor or digital signal processor" in which the encoder 12 is implemented. Thus, as neither Eifrig nor Pian discloses or suggests separate processors, the combination of Eifrig and Pain fails to disclose or suggest separate processors.

The proposed combination of Eifrig and Pian fails to disclose or suggest each and every feature recited by claims 13, 44 and 53

Independent claim 13 presently recites the features of "a memory", "a first processor to parse received video data to generate a plurality of packets and provide the plurality of packets for storage in the memory, the first processor comprising a general purpose processor," and "a second processor to access packets of the plurality of packets from the memory, the second processor including a video transcoder to transcode video data of the packets." The Office asserts that element 10 ("parsing/demux 10") of FIG. 1 of Eifrig represents the claimed "first processor" feature and further that element 30 ("core transcoding 30") of FIG. 1 of Eifrig represents the claimed "second processor" feature and further asserts that Pian would render it obvious to separate the element 10 and the element 30 into a first processor and a second processor, respectively. As discussed above, one of ordinary skill in the art will recognize that the parsing/demux (element 10) and the corresponding core transcoder (element 30)

conventionally are implemented together as a single processor and Pian fails to disclose or suggest the implementation of these elements in separate processors as provided by claim 13.

Further, claim 13 provides that the first processor is to parse received video data to generate a plurality of packets and provide the plurality of packets to the memory. Eifrig fails to disclose that its element 10 (which the Office equates to the claimed first processor) packetizes video data into packets and then stores the packets in memory. Pian likewise fails to disclose or suggest that the preprocessor 10 (which the Office equates to the claimed first processor) is connected to a memory or provides packets to a memory in any manner. *See, e.g., Pian*, col. 4, lines 6-7 ("The output of the preprocessor 10 is presented to the encoder 12"). Claim 13 also provides that the second processor is to access packets from the memory and includes a transcoder to transcode the packets. Eifrig fails to disclose or suggest that the element 30 accesses packets from memory for transcoding and Pian fails to disclose or suggest that the encoder 12 (which the Office equates to the claimed second processor) accesses packets from a memory.

Claim 13 also provides that the first processor is a general purpose processor, where the present application provides that "[a] general purpose processor is a data processor that performs one or more functions specified by software, where it is understood that software would include firmware." *Present Application*, p. 10, lines 29-31. Other than merely asserting that element 10 "is a general purpose element," the Office fails to establish that Eifrig teaches that the element 10 is a general purpose processor. Eifrig provides no disclosure that the parsing/demux element (element 10) "performs one or more functions specified by software." Moreover, one of ordinary skill in the art would appreciate that the element 10 of Eifrig would be implemented solely as hardware (e.g., a state machine) rather than as a general purpose processor. With respect to Pian, as discussed above, Pian fails to disclose or suggest a first processor and a second processor as recited by claim 13. For at least the reasons provided above, it is respectfully submitted that the proposed combination of Eifrig and Pian fails to disclose or suggest each and every feature recited by claim 13.

Independent claim 53 recites the features of: "receiving, at a first processor, a data stream including video data," "parsing, *at the first processor*, the data stream to identify video data

associated with a first channel," "packetizing, *at the first processor*, the video data associated with the first channel to generate the one or more packets, each packet having a video data payload and information related to the video data payload, wherein the video data payloads of the one or more packets represent a first channel of compressed video data having a characteristics represented by a first value," "*storing the one or more packets at a memory*", "*accessing*, at a second processor, the one or more packets *from the memory*," and "transcoding, *at the second processor*, the video data payloads of the one or more packets to generate a representation of a second channel of compressed video data having the characteristic represented by a second value." As with claim 13, the Office asserts that element 10 ("parsing/demux 10") of FIG. 1 of Eifrig represents the first processor at which the claimed receiving, parsing, and packetizing operations are performed and that element 30 ("core transcoding 30") of FIG. 1 of Eifrig represents the second processor at which the claimed receiving and transcoding operations are performed, and further alleges that Pian teaches the implementation of these components as separate processors. However, as similarly discussed above with respect to claim 13, the Office's interpretation of element 10 and element 30 of FIG. 1 of Eifrig or the preprocessor 10 and the encoder 12 of Pian as two separate processors is suggested solely by the present application and finds no support in the disclosure of Eifrig or Pian or in the knowledge of one of ordinary skill in the art at the time of the invention. Further, Eifrig fails to disclose or suggest the element 10 packetizes the video data and stores the packets in a memory, or that the element 30 accesses the packets from the memory as provided by claim 53. Likewise, Pian fails to disclose or suggest that the preprocessor 10 packetizes the video data and store the packets in a memory, or that the encoder 12 accesses the packets from the memory as provided by claim 53. Accordingly, the proposed combination of Eifrig and Pian fails to disclose or suggest the above-identified features of claim 53.

Independent claim 44 presently recites the features of "a *memory*", "a first data processor to: *access one or more packets* having a video data payload and information related to the video data payload *from the memory*, wherein the video data payloads of the one or more packets represent a first channel of compressed video data having a characteristic represented by a first value; and transcode the video data payloads of the one or more packets to generate a representation of a second channel of compressed video data having the characteristic represented by a second value" and "*a second data processor comprising a general purpose*

processor, the second data processor to: receive a data stream including video data at a first data processor; parse the data stream to identify video data associated with a first channel; packetize the video data associated with the first channel to generate the one or more packets; and *provide the one or more packets for storage in the memory*." As discussed above, Eifrig and Pian fail to disclose or suggest one data processor to parse and packetize video data and a separate processor to transcode the parsed and packetized video data. Eifrig and Pian also fails to disclose or suggest that the element 10/preprocessor 10 stores packets in memory and that the element 30/encoder 12 accesses the packets from memory for processing. The proposed combination of Eifrig and Pian therefore fails to disclose or suggest the claimed first and second data processor features recited by claim 44.

The proposed combination of Eifrig and Pian fails to disclose or suggest a second processor coupled to a first processor through a memory controller and a sequencer as recited by claim 29

Dependent claim 29 recites the features of "wherein the second processor is coupled to the first processor through a memory controller and a sequencer." With respect to these features, the Office merely states "wherein the second element is coupled to the first element through a memory controller and a sequencer (col. 6, ln. 6-41 [of Eifrig]) as specified in claim 29" and provides no further support for its rejection of claim 29. *See Office Action*, p. 3. It is respectfully submitted that the Office fails to establish how Eifrig discloses a memory controller and a sequencer (much less that they couple two processors) and thus the Office fails to meet its burden of establishing a *prima facie* case of obviousness with respect to claim 29. For example, if the Office identifies element 10 also as the first processor, so it is not understood how a first processor (allegedly element 10) can be coupled to a second processor through itself (allegedly through elements 10 and 20). Moreover, it is not understood how elements 10 and 20 constitute a memory controller and a sequencer.

Conclusion

The Applicants respectfully submit that the present application is in condition for allowance, and an early indication of the same is courteously solicited. The Examiner is respectfully requested to contact the undersigned by telephone at the below listed telephone number in order to expedite resolution of any issues and to expedite passage of the present

application to issue, if any comments, questions, or suggestions arise in connection with the present application.

The Commissioner is hereby authorized to charge any fees that may be required, or credit any overpayment, to Deposit Account Number 50-1835.

Respectfully submitted,

/Ryan S. Davidson/ March 21, 2008
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